CT1800 / CT1801

Protocol/Subsystem Interface Hybrid for MIL-STD-1553B

July 1985

Advance Information

005356

Features

- Final link in 1553B to subsystem interface effectively translates 1553B requirements into simple µP "peripheral" requirements.
- Subsystem receives and transmits data as if it was reading or writing to a typical µP port-type device.
- Unique circuit design prevents erroneous data from reaching the 2K x 16 RAM.
- The command word and all data words are verified before the subsystem is notified of a new message.
- Provides 2K of dual-ported double-buffered RAM internally partitioned as 30 receive buffers and 30 transmit buffers — memory mapped by subaddress.
- All transfer of data resulting from "Transmit Data" command is independent of subsystem — frees subsystem µP.
- No timing or handshaking signals to generate or decode — all are self-contained between Protocol Hybrid and CT1800/CT1801.
- Minimizes "glue logic" interface with any microprocessor.
- No critical timing imposed on microprocessor subsystem.
- Pin programmable for 8-bit and 16-bit microprocessors.
- Unlimited number of single, dual, tri or quad redundant RTU's may be designed into or later added on to an existing microprocessor bus.
- All CMOS for low-power and high-speed.

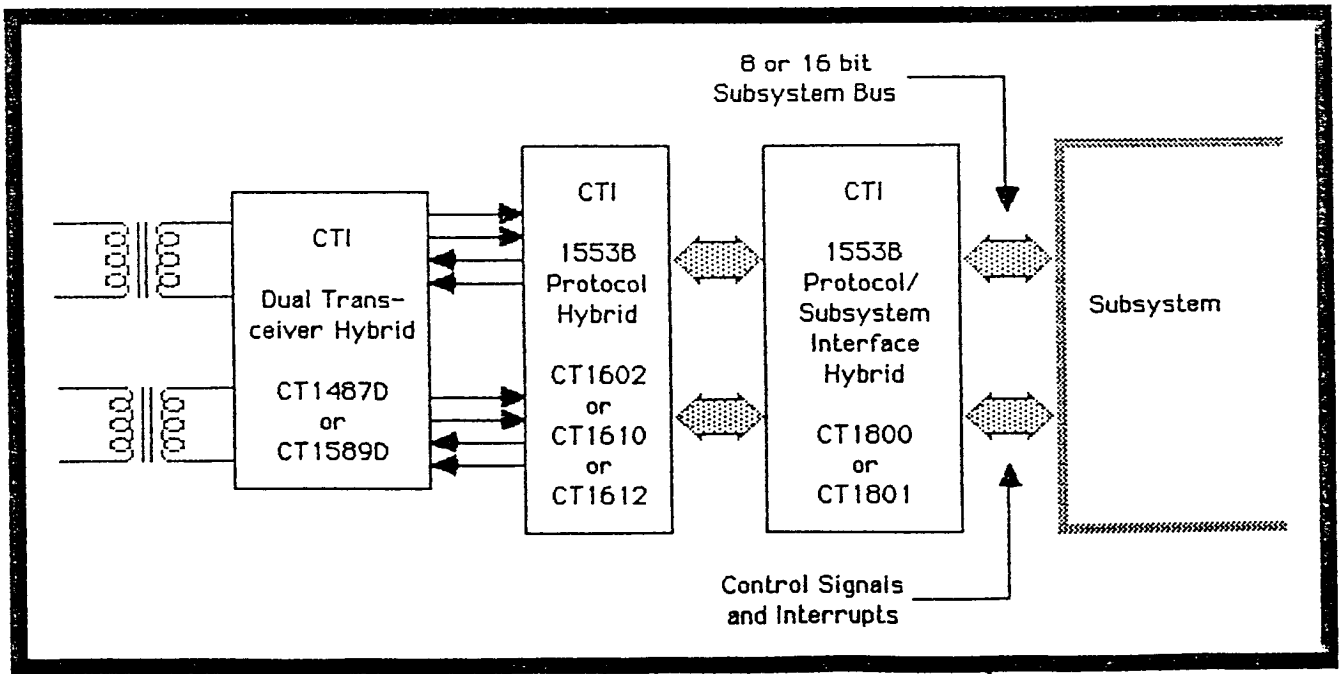

Fig. 1 — System Configuration

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PRELIMINARY

CT1800/1801
MIL-STD-1553B RTU TO MICROPROCESSOR INTERFACE

Key Features

* No critical timing imposed on microprocessor subsystem
* Minimizes "Glue Logic" interface with any microprocessor
* Provides 2K of dual ported double buffered RAM internally partitioned as 30 receive buffers and 30 transmit buffers, memory mapped by subaddress
* Pin programmable for 8 and 16 bit microprocessors
* All HCMOS for low power and high speed
* Unlimited number of single, dual, tri or quad redundant RTU's may be designed into or later added on to an existing microprocessor bus

General

The CT1800/CT1801 provides a complete remote terminal interface between the Circuit Technology MIL-STD-1553B protocol chip set (CT1561, CT1610, CT1612 etc.) and any microprocessor subsystem. Figure 1 illustrates a system configuration. This interface completely separates the RTU from the subsystem by providing all data buffers and control registers. Internal arbitration and data transfer control circuitry eliminates subsystem response requirements. All data written into or read from this interface is double buffered on a message basis. Only valid and complete receive messages are transfered into the receive RAM.

The CT1800/CT1801 interface supports all 15 mode codes and all types of data transfers allowed by MIL-STD-1553B. The CT1800 and CT1801 are identical in all respects except that the CT1801 does not contain the 2Kx16 message RAM internally. This permits the use of non-volatile RAM and other memory configurations with the interface.

All active components in the CT1800/CT1801 are HCMOS which results in very low power requirements. This includes FIFO, RAM, and custom integrated circuits.

Interfacing to the subsystem is simplified via the use of a tri-stated input/output data bus. Control signals basically consist of four address lines, a device select input, read strobe, write strobe and several interrupts, the use of which are optional.

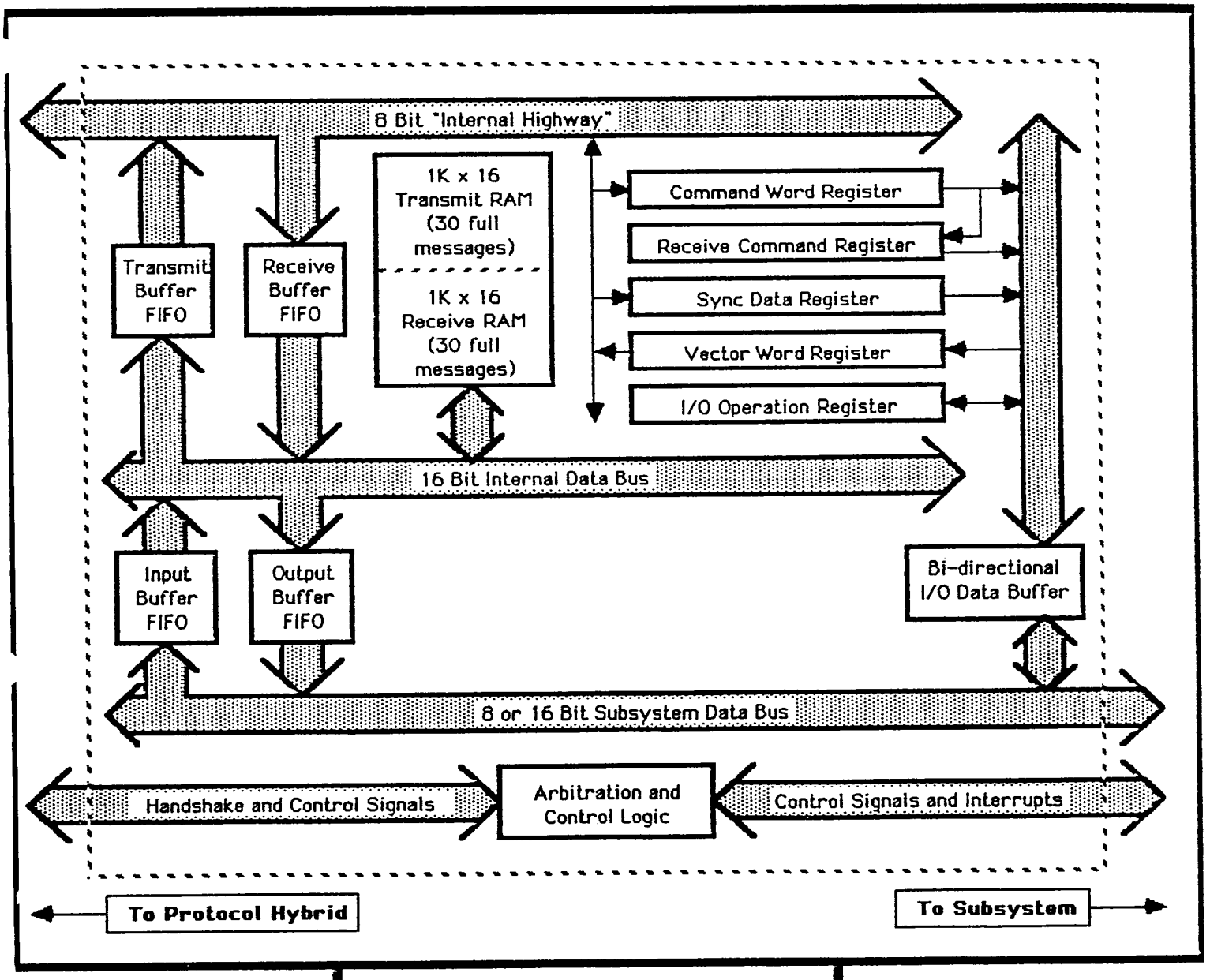


Fig. 2 — Functional Block Diagram

Note 1: Receive Command register is a double-buffered version of the Command Word register. This maximizes subsystem access time.

Note 2: Input and Output FIFO buffers hold one message each to provide double-buffering of data on a message basis.

Operation

Figure 2 is a block diagram of the CT1800. This figure shows that there are three independent parallel data buses within the hybrid. Separating these buses are XMIT, RCV, INPUT and OUTPUT FIFO Buffers. The first bus is the Internal Highway. This 8 bit wide bus is the data path where all transfers to or from the protocol chip set (i.e. CT1610) front end take place. The eight bit width minimizes system interconnections. It is separated from the second bus, the Internal Data Bus by the XMIT and RCV FIFO buffers. This permits data transfers on the Internal Data Bus to be independent of data transfers on the Internal Highway. The Internal Data Bus is 16 bits wide and permits high speed block data transfers between the 2Kx16 RAM message buffer and any of the four FIFO buffers. The third bus is the Subsystem Data Bus. It is separated from the Internal Data Bus by the INPUT and OUTPUT FIFO buffers. The Subsystem Data Bus is pin programmable for either 8 or 16 bit width to accommodate 8 or 16 bit microprocessor subsystems.

Data transfers on the Internal Data Bus and the Internal Highway are transparent to the subsystem. Transfers on either bus are elicited in response to a 1553B command. Transfers on the Internal Data Bus are also elicited by subsystem command. Arbitration of the data transfers is resolved internally and is transparent to the subsystem.

Subsystem data transfers are accomplished by either reading or writing to the INPUT or OUTPUT FIFO buffers as I/O ports. Data is transferred from the internal RAM to the OUTPUT buffer via a single I/O command. Data loaded into the INPUT buffer is transferred to the internal RAM via a single I/O command.

Five registers are provided for the command words, mode data words and interface operation. These registers are always accessible to the subsystem.

The Receive Command Word Register is double buffered to maximize the access time provided to the subsystem before a new receive command word can overwrite it.

Receive Command Service

When a valid receive command is sent to the RTU the command word is first loaded into the Command Word Register. As the data words associated with this command are received they are loaded one by one into the RCV FIFO buffer. Once the entire message is received and validated the command word is transferred to the RCV Command Register. The entire block of data is then burst into the corresponding subaddress message block of the receive section of the internal RAM. Once this operation is complete a discrete interrupt pulse called GOOD BLOCK is sent the subsystem.

Appropriate subsystem response to the interrupt would be to read the command word from the RCV Command Register. The data may then be transferred to the OUTPUT FIFO buffer, and read by the subsystem. Each receive subaddress section of the internal RAM will contain only the most recent valid and complete block of data transmitted to the RTU from the Bus Controller.

Transmit Command Service

When a valid transmit command is sent to the RTU, the command word is loaded into the Command Word Register. The block of data corresponding to the subaddress of the transmit command is then burst transferred from the internal RAM to the XMIT FIFO buffer. The data is then transferred word by word onto the 1553B bus. Once the transmit data has been transferred to the buffer the interrupt pulse VAL TRANS is sent to the subsystem.

The transmit section of the internal RAM is generally initialized at power up (reset) and periodically updated as required.

Appropriate subsystem response to the transmit interrupt may be to read the command word from the Command Word Register or simply reset an internal timer that verifies the 1553B bus is active.

Since updates to the internal RAM are made on a message basis there is never the possibility that new and old data are mixed. Only the last complete message at any subaddress is transmitted.

Mode Code Service

All 15 mode codes are serviced by the protocol chip set front end and most do not require any subsystem intervention. Discrete interrupt pulse signals are available for each of the synchronize (with and without data) Vector Word, Reset and Dynamic Bus Control Acceptance mode codes. Mode command words are loaded into the Command Word Register. Separate registers are provided for the synchronize data word and the vector data words.

Discrete Interrupts

Eight discrete interrupt output signals are available for the subsystem interface. Any or all of these may be used depending on subsystem requirements. All of the interrupts are low going pulse signals. The empty flag for the output buffer BUFFEF is also made available to the subsystem. When high it indicates the output buffer is not empty. All of the pulse interrupts are 160 nsec (NOM) wide except for RESET and DBREQ which are 500 nsec (NOM). These two interrupts are generated directly from the protocol front end and not the CT1800.

The interrupt functions are summarized in the table below.

DISCRETE INTERRUPTS

Name	Type	Use
$\overline{\text{GOOD BLOCK}}$	160 nsec pulse	INDICATES VALID RECEPTION of valid block of data. The RECEIVE COMMAND WORD is loaded in RCV CMD WD Register. This interrupt is issued after the new block of data is moved into the Internal RAM.
$\overline{\text{VALID TRANS}}$	160 nsec pulse	INDICATES VALID RECEPTION of TRANSMIT COMMAND WORD. The TRANSMIT COMMAND WORD is loaded in CMD WD Register. Note: This interrupt does not necessarily indicate that the transmitted data was received by the bus controller.
$\overline{\text{SYNC NO DATA}}$	160 nsec pulse	INDICATES VALID RECEPTION of mode command SYNCRONIZE WITHOUT DATA. MODE COMMAND WORD loaded in CMD WD register.
$\overline{\text{SYNC W/DATA}}$	160 nsec pulse	INDICATES VALID RECEPTION of mode command synchronize with DATA. Mode command word is loaded in CMD WD register. SYNCRONIZE data word is loaded in the SYNC DATA REGISTER. This interrupt will not be issued if a word count high or low error occurs.

DISCRETE INTERRUPTS (CONT'D)

NAME	TYPE	USE
$\overline{\text{DONE}}$	160 nsec pulse	This interrupt is issued in response to an I/O command from the subsystem. In response to an I/O load OUTPUT buffer command it indicates that the complete 32 word message block (SUBADDRESS) has been loaded into the OUTPUT FIFO buffer. In response to an I/O load internal RAM from INPUT buffer command it indicates the full message (1 to 32 WORDS) has been loaded. TIMING a. In response to an I/O load OUTPUT buffer: 16.5 to 33 usec* b. In response to an I/O load RAM from INPUT buffer: 16.5 to 33 usec for 32 WORDS*, for SHORTER LOAD OPERATIONS SUBTRACT .5 usec per (16 bit) word i.e. .5 usec to 17 usec for single word. *NOTE: In the unusual case where a superceding transmit command on the redundant bus occurs at the returned status time for a valid 32 word receive, simultaneously with an I/O transfer request the DONE interrupt may be delayed for an additional 16.5 usec.
$\overline{\text{BUFF EF}}$	flag	This flag may be used to speed up read data operation in response to an I/O load OUTPUT buffer command. The BUFF EF flag will go high when the first word is loaded into the OUTPUT FIFO buffer. This word may be read at this time . Since the output buffer is loaded internally at .5 usec/WORD rate and the minimum I/O read time is .5 usec/WORD, continuous I/O read operations may then be initiated. Use of this flag may save up to 16.5 usec in subsystem interface protocol.

DISCRETE INTERUPTS (CONT'D)

NAME	TYPE	USE
$\overline{\text{RESET}}$	.5usec pulse (From CT1610/12)	INDICATES VALID RECEPTION of the RESET mode command. RESET mode command word is contained in CMD WD REGISTER.
$\overline{\text{VECTEN}}$	1.5 usec pulse. (From CT1610/12)	INDICATES that VALID transmit VECTOR mode command has been received. VECTOR DATA is transmitted from VECTOR REGISTER, COMMAND WORD is located in CMD WD REGISTER.
$\overline{\text{DBCREQ}}$	.5 usec pulse. (From CT1610/12)	INDICATES ACCEPTANCE OF DYNAMIC BUS CONTROL COMMAND REQUEST. Command Word is located in CMD WD Register. NOTE: RTU will not accept valid DBC mode command unless DBCACC signal is set low in 1553B protocol front end.

In addition to the interrupts and flag given in the table above, the NBGT signal (.5 usec pulse) may be used in the subsystem interface. When this signal pulses it indicates the reception of a non specific valid command word. It may be used to monitor bus activity.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE V_{DD}	-.3V to +7.0
INPUT OR OUTPUT VOLTAGE ON ANY PIN	-.3V to V_{DD} +.3V
MAXIMUM CURRENT THROUGH ANY SIGNAL PIN	10mA
STORAGE TEMPERATURE	-55°C to +155°C

POWER DISSIPATION

MAXIMUM STAND BY CURRENT (QUIESENT)	50mA
MAXIMUM AVERAGE ACTIVE CURRENT	200mA
MAXIMUM POWER DISSIPATION	1W
WORST CASE COMPONENT ACTIVE POWER DISSIPATION	334mW
WORST CASE COMPONENT THERMAL RESISTANCE (Θjc)	9.6°C/W
WORST CASE COMPONENT THERMAL RISE ABOVE CASE	3.2°C

RECOMMENDED DC OPERATING CONDTIONS

OPERATING SUPPLY VOLTAGE, V_{DD}	5.0V +/- 10%
OPERATING AMBIENT TEMPERATURE (CASE), T_C	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (Vdd = 5.0V ± 10%; -55°C ≤ T_A ≤ +125°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	INPUT LOGIC "1"	2.2			V_{DC}	
V_{IL}	INPUT LOGIC "0"			.8	V_{DC}	
I_{IN}	INPUT CURRENT			25	uA	
V_{OH}	OUTPUT LOGIC "1"	2.4			V_{DC}	I_{OH} = -1mA
V_{OL}	OUTPUT LOGIC "0"			.4	V_{DC}	I_{OL} = 3mA
C_{IN}	INPUT CAPACITANCE			15	pF	
C_O	OUTPUT CAPACITANCE			20	pF	

MICROPROCESSOR INTERFACE

The CT1800/1801 is pin programmable to accomodate 8 and 16 BIT DATA BUS WIDTHS. Figure illustrates a typical 16 BIT INTERFACE. Figure illustrates a typical 8 BIT INTERFACE. Note that the 8 BIT INTERFACE has the HIGH ORDER data bus bits wired to their corresponding LOW ORDER bits.

In the 16 BIT MODE all registers and the input output buffers are READ and WRITTEN to on a word basis. In the 8 BIT MODE all registers are READ and WRITTEN to on a high or low BYTE basis. The input and output buffers are read and written to in a serial byte basis where the high BYTE is either written or read first.

SUMMARY OF REGISTERS

REGISTER NAME	FUNCTION
OPERATION	SPECIFIES INPUT/OUTPUT OPERATION INCLUDES: SUBADDRESS TRANSMIT/RECEIVE LOAD/UNLOAD RAM BLOCK ALSO INCLUDES BUSY BIT, WHICH IS SET BUSY WITH MASTER RESET, i.e., AT POWER UP. (READ AND WRITE)
CMD WD	CONTAINS LAST VALID COMMAND WORD. (READ ONLY)
RCV CMD WD	CONTAINS LAST VALID RECEIVE COMMAND WORD. DOUBLE BUFFERED COPY OF CMD WD REGISTER. (READ ONLY)
SYNC DATA	CONTAINS SYNCHRONIZE DATA WORD ASSOCIATED WITH VALID SYNCHRONIZE WITH DATA MODE COMMAND. (READ ONLY)
VECTOR WD	CONTAINS VECTOR DATA WORD TO BE TRANSMITTED IN RESPONSE TO VALID RECEPTION OF VECTOR MODE COMMAND. (WRITE ONLY)

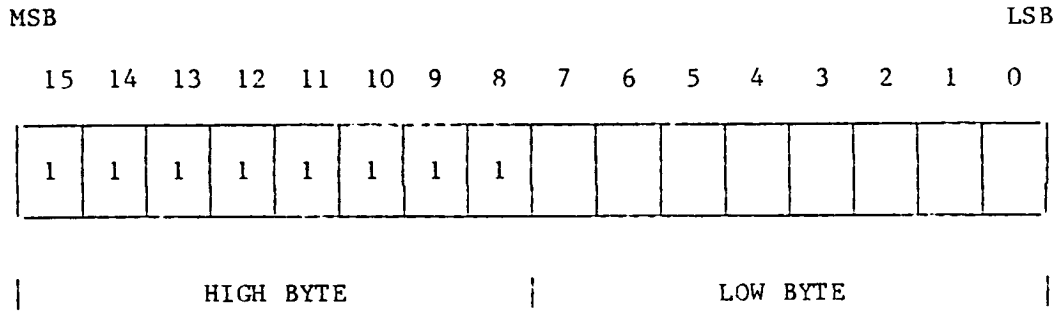
OPERATION REGISTER

The OPERATION REGISTER contains the information provided by the microprocessor subsystem for writing data to or reading data from the INTERNAL RAM. The INTERNAL RAM is divided into transmit and receive sections. In general, data is written to the transmit section and read from the receive section. However either section may be read from or written to via the T/R BIT in this register. In addition, this feature may be defeated so that the receive and transmit sections coincide both to the 1553B side and the subsystem side.

Bit 7 of the REGISTER is the Busy Bit. When the interface is reset, such as at power up, this bit is set so the RTU will respond busy.

The I/O TRANSFER FUNCTIONS defined by this register are executed by either of the two EXECUTE COMMANDS.

OPERATION REGISTER



1. RESET TO $FF80_H$

2. ADDRESS CODE = 0000_B (16 BIT MODE)
   0000_B (LOW BYTE, 8 BIT MODE)
   0001_B (HIGH BYTE, 8 BIT MODE)

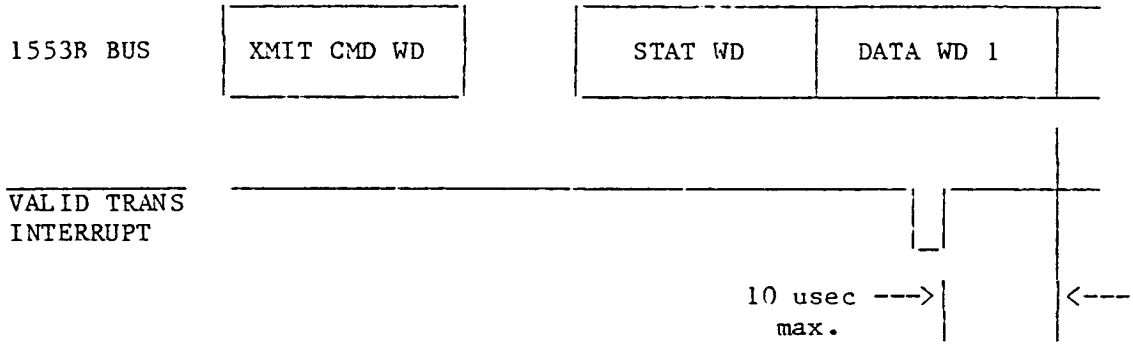
BIT	NAME	FUNCTIONS
0-4	SA BITS	SUBADDRESS BITS Define SUBADDRESS MESSAGE BLOCK in INTERNAL RAM. BIT / SUBADDRESS BIT 0 — SA 0 (LSB) 1 — SA 1 2 — SA 2 3 — SA 3 4 — SA 4 (MSB) These bits correspond directly to 1553B definition in command word. Although SUBADDRESSES 00000_B AND 11111_B are illegal in 1553B, message blocks specified by them are both READABLE and WRITABLE by the SUBSYSTEM. They are not accessable from the 1553B BUS.

BIT	NAME	FUNCTION
5	T/$\overline{R}$ BIT	TRANSMIT/RECEIVE BIT points INPUT/OUTPUT OPERATION to either the TRANSMIT SECTION or RECEIVE SECTION of the INTERNAL RAM.
6	I/$\overline{O}$ BIT	INPUT/OUTPUT BIT DEFINES DIRECTION OF DATA TRANSFER 1. SET HIGH: INPUT OPERATION Data currently loaded in the input FIFO BUFFER is moved to the specified message block (SUBADDRESS) in the INTERNAL RAM. If EXECUTE with RPT OPTION COMMAND is used, previously loaded data (i.e. data for which a load operation was previously executed) will be loaded to a new message block. Between 1 and 32 data words must be loaded in the input FIFO BUFFER when using an EXECUTE command with this bit set. 2. SET LOW: OUTPUT OPERATION When set low the execute operation will transfer a complete block of data (32 words) to the output FIFO buffer from the specified subaddress of internal RAM.
7	BUSY BIT	RTU BUSY HIGH = BUSY LOW = NOT BUSY MASTER RESET SETS BIT HIGH
8-15	RESERVED	RESERVED All bits set high

COMMAND WORD REGISTER (CMD WD)

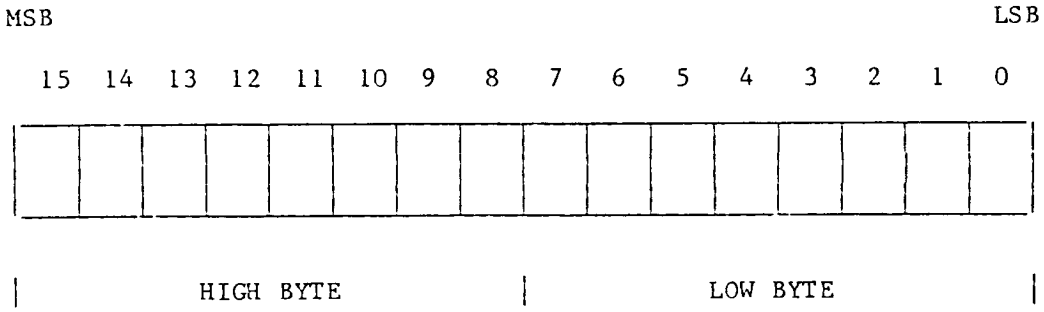
The COMMAND WORD REGISTER contains the last valid command received by the RTU. While this includes receive command words, the subsystem should be designed to read only TRANSMIT and MODE commands from this register. RECEIVE commands should be read from the RCV CMD register which is a double buffered version of this register.

In general, the only time the subsystem may need to read this register is in response to a VALID TRANSMIT COMMAND. This would be in the case where the subsystem needed to know the subaddress and word count of the command. The VALID TRANSMIT interrrupt will be pulsed no later than 10 usec before the end of the first transmitted data word as shown in the figure below.



The maximum subsystem access time for this register is the minimum time interval after which a new command word may be received. Individual interrupts are given for each of the MODE codes that might require subsystem action, the subsystem therefore does not need to read this register for MODE codes.

COMMAND WORD REGISTER (CMD WD)



1. RESET TO 0000_H

2. ADDRESS CODE = 0100_B (16 BIT MODE)
   0100_B (LOW BYTE, 8 BIT MODE)
   0101_B (HIGH BYTE, 8 BIT MODE)

BIT	NAME	FUNCTION
0-4	WC/MC FIELD	WORD COUNT/ MODE CODE FIELD 1. FOR DATA TRANSFERS WC/MC = WORD COUNT NOTE: 00000_B = 32 WORDS 2. FOR MODE COMMANDS WC/MC = MODE CODE SPECIFICATION
5-9	SA/M FIELD	SUBADDRESS/MODE FIELD When DATA transfers, this field is the SUBADDRESS field in the INTERNAL RAM. However when field is 00000_B or 11111_B it specifies that the command is a MODE COMMAND.

COMMAND WORD REGISTER (CONT'D)

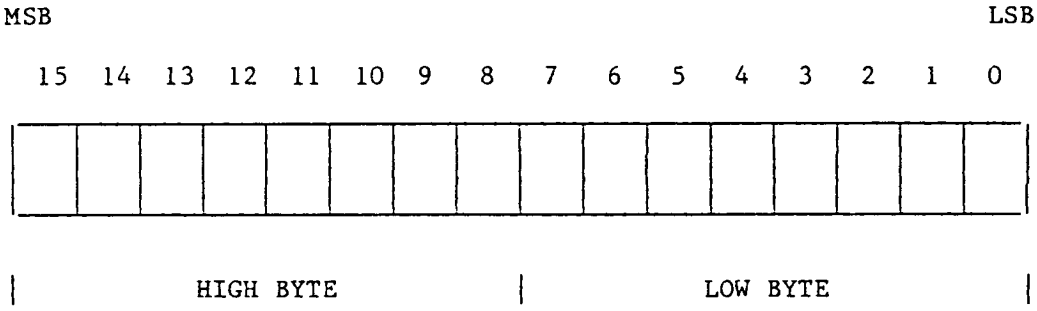
BIT	NAME	FUNCTION
10	TX/$\overline{RX}$	TRANSMIT/RECEIVE BIT
11-15	RTAD	RTU ADDRESS FIELD This field will contain only the HARD WIRED RTU ADDRESS or the BROADCAST ADDRESS (11111_B) if the RTU is enabled to receive BROADCAST COMMANDS. Reception of BROADCAST COMMANDS is enabled by a HIGH on the BCSTEN1 and BCSTEN0 input signal pins of the protocol front end.

RECEIVE COMMAND REGISTER (RCV CMD)

The RECEIVE COMMAND REGISTER contains the last valid receive command received by the RTU. It is a doubled buffer version of the COMMAND WORD REGISTER. This maximizes the time provided to the subsystem for reading the receive command before any new command can overwrite it.

Generally, the subsystem would read this register after the GOOD BLOCK interrupt issued.

RECEIVE COMMAND REGISTER (RCV CMD)



1. RESET TO 0000_H

2. ADDRESS CODE = 0010_B (16 BIT MODE)
   0010_B (LOW BYTE, 8 BIT MODE)
   0011_B (HIGH BYTE, 8 BIT MODE)

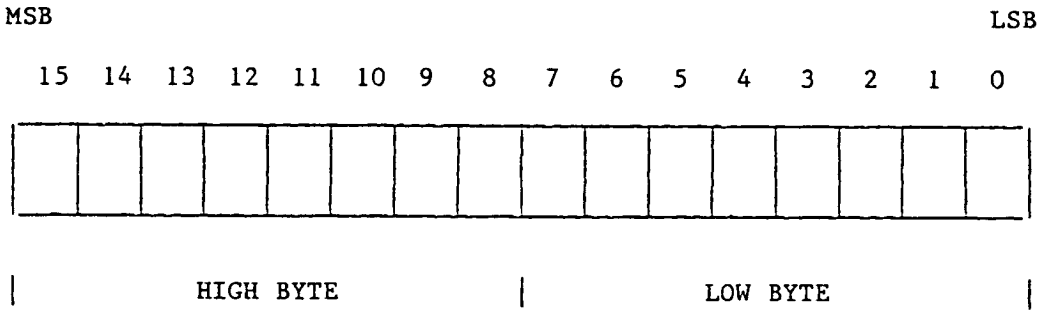
BIT	NAME	FUNCTION
0-4	WC FIELD	WORD COUNT FIELD NOTE: 00000_B = 32 WORDS
5-9	SA FIELD	SUBADDRESS FIELD NOTE: NEVER 00000_B OR 11111_B
10	TX/$\overline{RX}$	TRANSMIT/RECEIVE BIT ALWAYS SET LOW (0)
11-15	RTAD	RTU ADDRESS FIELD This field will contain only the HARD WIRED RTU ADDRESS or the BROADCAST ADDRESS (11111_B) if the RTU is enabled to receive BROADCAST COMMANDS. Reception of BROADCAST COMMANDS is ENABLED by a HIGH on BCSTEN1 and BCSTEN 0 input signal pins of the PROTOCOL FRONT END.

SYNCHRONIZE DATA REGISTER (SYNC DATA)

The SYNCHRONIZE DATA REGISTER contains the last received mode data word associated with the SYNCHRONIZE WITH DATA MODE COMMAND. This register is read only from the subsystem.

Generally, the subsystem would read this register after the SYNC W/DATA INTERRUPT IS ISSUED.

SYNCHRONIZE DATA REGISTER (SYNC DATA)



1. RESET TO 0000_H

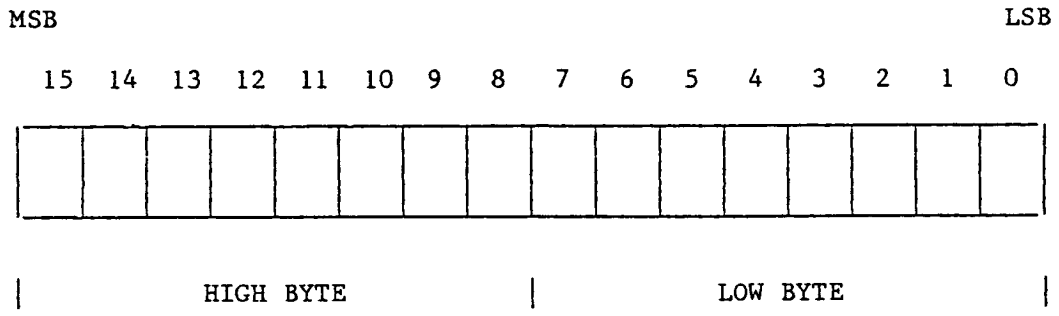
2. ADDRESS CODE = 0110_B (16 BIT MODE)
   0110_B (LOW BYTE, 8 BIT MODE)
   0111_B (HIGH BYTE, 8 BIT MODE)

VECTOR WORD REGISTER

The VECTOR WORD REGISTER provides the data transmitted from the RTU in response to the mode command TRANSMIT VECTOR WORD. This register is write only from the subsystem. In some 1553B systems the VECTOR word is used to specify the particular service requested of the BUS CONTROLLER by the RTU, when the RTU sets the SERVICE REQUEST bit in the STATUS word. In such systems the VECTOR WORD is loaded before the SERVICE REQUEST bit is set.

While the format of the VECTOR word is not specified by 1553B, a system may be designed where the content of the VECTOR word is the actual command word the BUS CONTROLLER will transmit to the RTU in response to the requested service.

VECTOR WORD REGISTER



1. RESET TO 0000_H

2. ADDRESS CODE = 0110_B (16 BIT MODE)
   0110_B (LOW BYTE, 8 BIT MODE)
   0111_B (HIGH BYTE, 8 BIT MODE)

SUBSYSTEM INTERFACE SIGNALS

The CT1800 and CT1801 provide simple interface signals that are intended to be connected to the address, data and control buses of the subsystem. The subsystem may address the interface as if it were an I/O device or memory.

The interface is compatable with systems that have short or no data hold time during write cycles such as the F9450A microprocessor. This was accomplished by incorporating a circuit that terminates the write cycle early (i.e before $\overline{WT}$ or $\overline{DS}$ return high). This effectively provides more hold time for the data. However, to take advantage of this feature the write cycle must be greater than 550 nsec. Systems providing data hold times of 50 nsec or greater may have write strobes as short as 350 usec.

SUBSYSTEM INTERFACE SIGNALS

SIGNAL NAME	FUNCTION
A0-A3	INPUT ADDRESS A0 = LSB A3 = MSB These four signals provide the address codes that control the operation of the interface.
$\overline{DS}$	DEVICE SELECT Used in conjunction with the address signals. The input/output interface data bus will remain tri-stated and no operation will be executed when this signal is high, regardless of the state of the address signals. $\overline{DS}$ = LOW (0) INTERFACE SELECTED $\overline{DS}$ = HIGH (1) INTERFACE NOT SELECTED
DB0-DBF	I/O DATA BUS Data bus for all SUBSYSTEM READ and WRITE OPERATIONS. 16 BIT MODE: DB0 = LSB; DBF = MSB 8 BIT MODE: DB0/DBB = LSB; DB7/DBF = MSB When used in 8 BIT MODE the data bus must be connected as follows: DB0 TO DB8 DB1 TO DB9 DB2 TO DBA DB3 TO DBB DB4 TO DBC DB5 TO DBD DB6 TO DBE DB7 TO DBF

SUBSYSTEM INTERFACE SIGNALS (CONT'D)

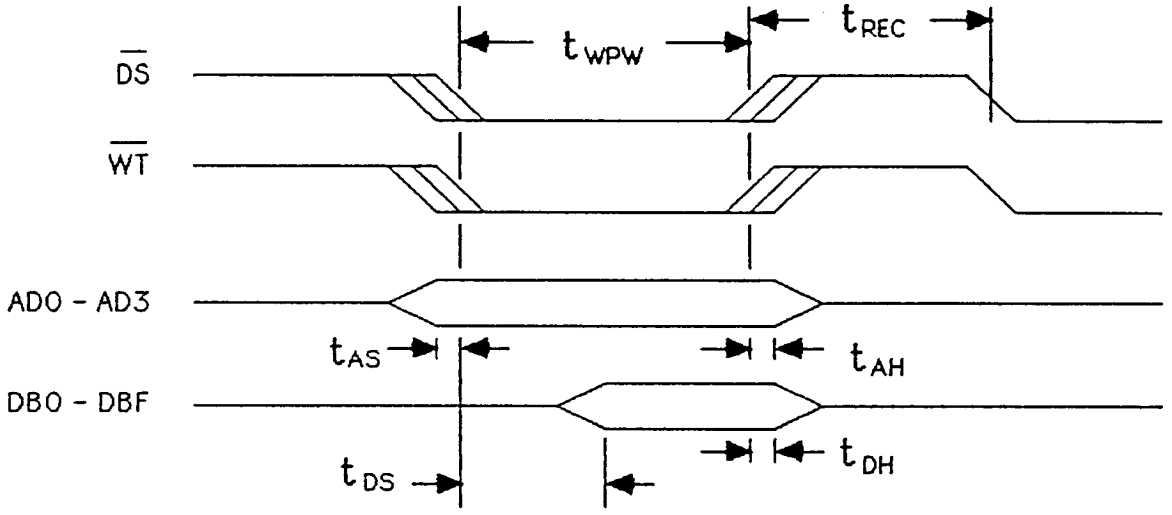
SIGNAL NAME	FUNCTION
16/$\overline{8}$	PROGRAMS INTERFACE FOR 8 BIT OR 16 BIT DATA BUSES 16/$\overline{18}$ = LOW (0) 8 BIT MODE 16/$\overline{18}$ = HIGH (1) 16 BIT MODE
$\overline{\text{MASTER RESET}}$	SYSTEM RESET When low resets all registers and INPUT/OUTPUT buffers. Minimum Low Time for reset = .5usec.
$\overline{\text{WT}}$	WRITE STROBE Must GO LOW together with $\overline{\text{DS}}$ to perform a WRITE OPERATION. NOTE: $\overline{\text{RD}}$ MUST BE HIGH
$\overline{\text{RD}}$	READ STROBE Must GO LOW together with $\overline{\text{DS}}$ to perform a READ OPERATION. NOTE: $\overline{\text{WT}}$ STROBE MUST BE HIGH.
INTERRUPTS	Refer to DISCRETE INTERRUPT TABLE

USE OF A10 AND A10IN (CT1800 ONLY)

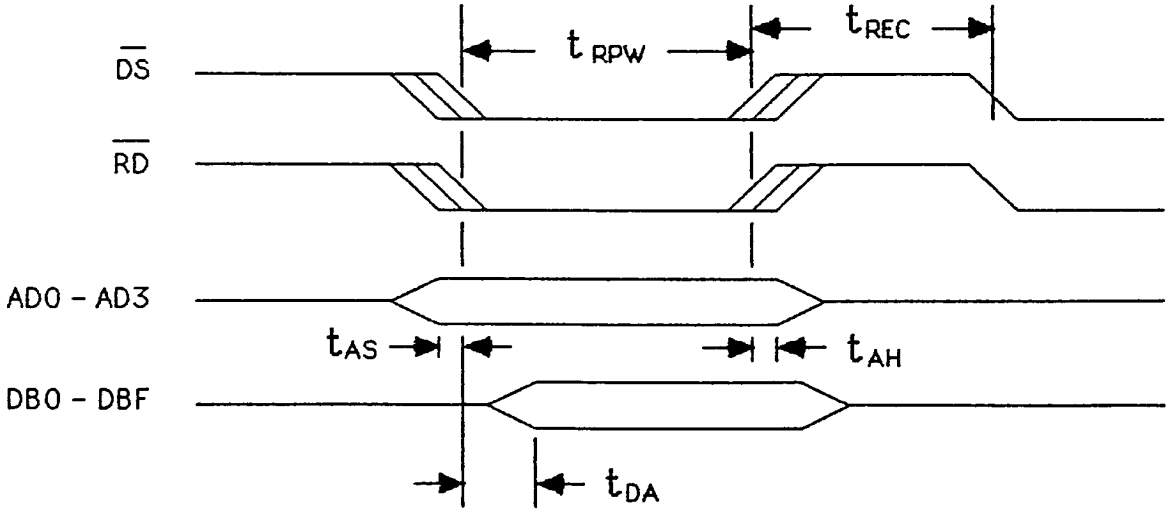
The standard configuration of the CT1800 divides the INTERNAL RAM into separate RECEIVE and TRANSMIT sections. For this configuration A10 is connected to A10IN. When A10 is high it addresses the TRANSMIT section, when low the RECEIVE sections. A10IN is the address input to the INTERNAL RAM.

The interface may be configured with one common section for both RECEIVE and TRANSMIT data. To configure this, A10 is not connected, and A10IN is fixed at either a logic high or low. If A10 and A10IN are not directly connected together but gated together (to permit switching between the standard and nonstandard configurations) then no more than 100 nsec of propogation delay should be introduced.

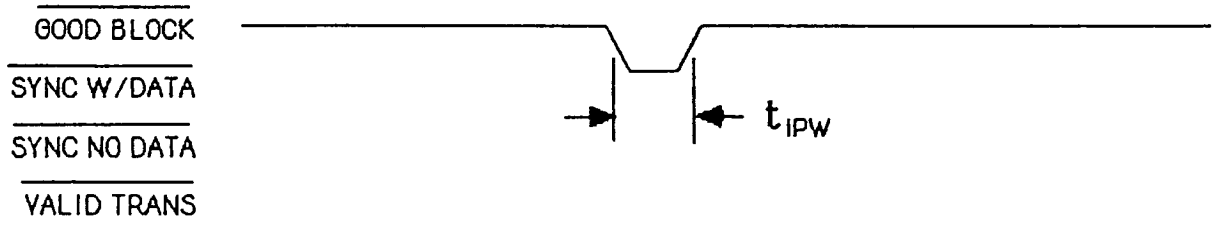
I/O Write Timing



I/O Read Timing



Output Interrupts



AC ELECTRICAL CHARACTERISTICS
($-55°C \leq T_A \leq +125°C$) V_{cc} = +5.0 VOLTS ± 10%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{WPW}	WRITE PULSE WIDTH	350			nsec	1,2
t_{RPW}	READ PULSE WIDTH	350			nsec	3
t_{AS}	ADDRESS SET UP TIME	5			nsec	
t_{AH}	ADDRESS HOLD TIME	5			nsec	
t_{DS}	WRITE DATA SET UP TIME			150	nsec	
t_{DH}	WRITE DATA HOLD TIME	0			nsec	2
t_{DA}	READ DATA ACCESS TIME			300	nsec	
t_{IPW}	INTERRUPT PULSE WIDTH	140	160	180	nsec	
t_{REC}	RECOVERY TIME	100			nsec	

NOTES:
1. Write pulse width t_{WPW} is the time when both $\overline{DS}$ and $\overline{WT}$ are simultaneously low. Either $\overline{DS}$ or $\overline{WT}$ may go low or return high first.
2. Write hold time: t_{DH} = 0 for $t_{WPW} \geq 550$ nsec
   t_{DH} = 50 nsec for 350 nsec < t_{WPW} < 550 nsec.
3. Read pulse time t_{RPW} is the time where both $\overline{DS}$ and $\overline{RD}$ are simultaneously low. Either $\overline{DS}$ or $\overline{RD}$ may go low or return high first.

INTERFACING THE CT1801

The only difference between the CT1800 and CT1801 is that the INTERNAL RAM is not physically located inside the hybrid. This permits configuration of the interface with external RAM memory. The tables below list the RAM interface signals:

RAM ADDRESS SIGNALS

ADDRESS BIT	FUNCTION NAME	COMMENTS
A0 A1 A2 A3 A4	CWC0 (LSB) CWC 1 CWC 2 CWC 3 CWC 4	CURRENT WORD COUNT These address bits point to each of the individual words in each subaddress message block.
A5 A6 A7 A8 A9	SA 0 SA 1 SA 2 SA 3 SA 4	SUBADDRESS These address bits point to each of the message subaddress blocks.
A10	TX/$\overline{RX}$ (MSB)	TRANSMIT/RECEIVE Points to transmit or receive section of ram buffer. LOW (0) = RECEIVE HIGH (1) = TRANSMIT NOTE: When using $\overline{CS1}$ or $\overline{CS2}$ data strobe signals, A10 is not used.

NOTE: A10IN IS NOT USED ON CT1801

RAM DATA BUS

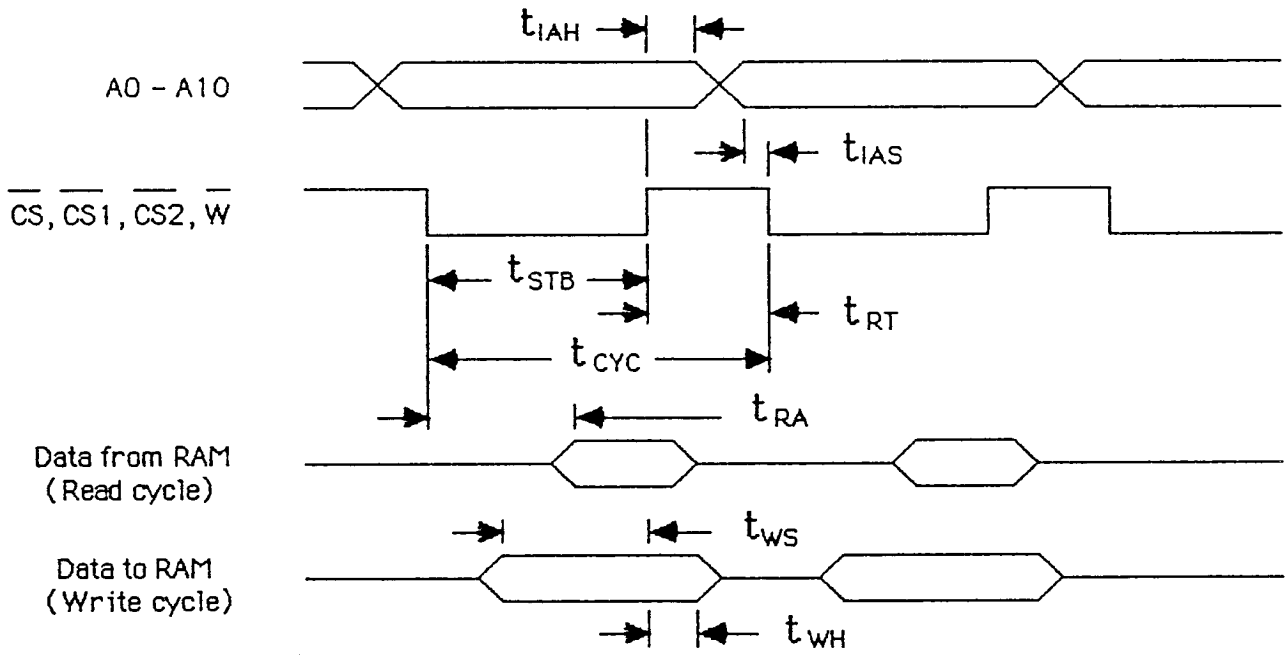
DATA BUS BIT	COMMENTS
IB0-IB15	INTERNAL DATA BUS IB0 = LSB IB15 = MSB All 16 data bus signals are internally pulled to ground through 10K (+/- 20%) resistors to prevent tri-stated bus from floating when not active.

RAM STROBE SIGNALS

SIGNAL	FUNCTION
$\overline{CS}$	CHIP SELECT This signal strobes for all data transfers read or write. Generally used with A10 when interfacing to 2KX8 RAM such as 6116 types.
$\overline{CS1}$	CHIP SELECT 1 This signal is identical to $\overline{CS}$ except it is active only when addressing the receive buffer. Generally used for interfacing to 1KX4 RAM such as 6514 types without A10.
$\overline{CS2}$	CHIP SELECT 2 This signal is identical to $\overline{CS}$ except it is active only when addressing the transmit buffer. Generally used for interfacing to 1KX4 RAM such as 6514 types without A10.
$\overline{W}$	WRITE This signal strobes for all write to RAM data transfers.

CT1801 EXTERNAL RAM
AC ELECTRICAL CHARACTERISTICS
($-55°C \leq T_A \leq +125°C$) V_{CC} = +5.0 VOLTS $\pm$ 10%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{IAH}	ADDRESS HOLD TIME	50	83		nsec
t_{IAS}	ADDRESS SET UP TIME	50	83		nsec
t_{STB}	STROBE PULSE WIDTH		333		nsec
t_{CYC}	CYCLE TIME		500		nsec
t_{RT}	RECOVERY TIME		166		nsec
t_{RA}	READ ACCESS TIME			250	nsec
t_{WS}	WRITE SET UP TIME	80			nsec
t_{WH}	WRITE HOLD TIME	25			nsec



External Ram Timing (CT1801 only)

16 BIT MODE I/O OPERATIONS

ADDRESS CODE							OPERATION
AD3	AD2	AD1	AD0	$\overline{WT}$	$\overline{RD}$	$\overline{DS}$	
X	X	X	X	X	X	1	NO OPERATION - I/O BUS TRI-STATED
0	0	0	0	1	0	0	READ OPERATION REGISTER
0	0	0	0	0	1	0	WRITE OPERATION REGISTER
0	0	1	0	1	0	0	READ RCV CMD REGISTER
0	1	0	0	1	0	0	READ CMD REGISTER
0	1	1	0	1	0	0	READ SYNC DATA REGISTER
0	1	1	0	0	1	0	WRITE VECTOR WORD REGISTER
1	0	0	0	0	1	0	EXECUTE OP. (LOAD/UNLOAD) RAM
1	0	1	0	0	1	0	EXECUTE OP. WITH RPT OPTION
1	1	0	0	0	1	0	RESET INPUT/OUTPUT BUFFERS
1	1	1	0	1	0	0	READ OUTPUT DATA BUFFER
1	1	1	0	0	1	0	WRITE INPUT DATA BUFFER

ALL I/O CODES NOT SPECIFIED ARE RESERVED.

8 BIT MODE I/O OPERATIONS

ADDRESS CODE							OPERATION
AD3	AD2	AD1	AD0	$\overline{WT}$	$\overline{RD}$	$\overline{DS}$	
X	X	X	X	X	X	1	NO OPERATION - I/O BUS TRI-STATED
0	0	0	0	1	0	0	READ OPERATION REGISTER LOW BYTE
0	0	0	1	1	0	0	READ OPERATION REGISTER HIGH BYTE NOTE: HIGH BYTE IS FIXED AT FF_H
0	0	0	1	0	1	0	WRITE OPERATION REGISTER LOW BYTE NOTE: HIGH BYTE IS NOT WRITABLE
0	0	1	0	1	0	0	READ RCV CMD REGISTER LOW BYTE
0	0	1	1	1	0	0	READ RCV CMD REGISTER HIGH BYTE
0	1	0	0	1	0	0	READ CMD REGISTER LOW BYTE
0	1	0	1	1	0	0	READ CMD REGISTER HIGH BYTE
0	1	1	0	1	0	0	READ SYNC DATA REGISTER LOW BYTE
0	1	1	1	1	0	0	READ SYNC DATA REGISTER HIGH BYTE
0	1	1	0	0	1	0	WRITE VECTOR WORD REGISTER LOW BYTE
0	1	1	1	0	1	0	WRITE VECTOR WORD REGISTER HIGH BYTE
1	0	0	0	0	1	0	EXECUTE OP. (LOAD/UNLOAD RAM)
1	0	1	0	0	1	0	EXECUTE OP. WITH RPT OPTION
1	1	0	0	0	1	0	RESET INPUT/OUTPUT BUFFERS
1	1	1	0	1	0	0	READ OUTPUT DATA BUFFER
1	1	1	0	0	1	0	WRITE INPUT DATA BUFFER

ALL I/O CODES NOT SPECIFIED ARE RESERVED.

NON-REGISTER OPERATIONAL COMMANDS

There are five operational commands that are not register read or write operations. These commands are summerized in the table below. The two execute operations are dependent on the contents of the OPERATION register. The address codes for all the operational commands are summarized in the 8 bit and 16 bit I/O OPERATIONAL tables.

NON-REGISTER OPERATIONAL COMMANDS

OPERATION	FUNCTION
RESET	RESET INPUT/OUTPUT BUFFERS This command clears both the input and output FIFO buffers. The BUFF EF flag will go low indicating the output buffer is empty.
READ OUTPUT DATA BUFFER	READ OUTPUT FIFO READS the data moved from the INTERNAL RAM in response to an UNLOAD execute operation. The order of the data words corresponds to the same order that they would be received on the 1553B bus. That is, the first data word read is the first data word following the COMMAND word. In 8 bit mode the high byte is read first.
WRITE INPUT DATA BUFFER	WRITE INPUT FIFO WRITES the data that will be moved into the INTERNAL RAM in response to a LOAD execute operation. The order of the data words corresponds to the same order that they would be transmitted on the 1553B bus. That is, the first data word written is the first data word transmitted following the STATUS word. In 8 bit mode the high byte is written first.

NON-REGISTER OPERATION COMMANDS

OPERATION	FUNCTION
EXECUTE OP.	EXECUTES OPERATION SPECIFIED IN OPERATION REGISTER 1. I/$\overline{O}$ BIT HIGH Data currently in INPUT FIFO BUFFER is loaded into the INTERNAL RAM block specified by the T/R BIT and SUBADDRESS FIELD of the OPERATION REGISTER. INPUT BUFFER must have at least one data word. The DONE interrupt is pulsed when the operation is completed. 2. I/$\overline{O}$ BIT LOW An entire block of data (32 words) specified by the T/R and the SUBADDRESS field of the OPERATION REGISTER is unloaded from the INTERNAL RAM into the OUTPUT FIFO BUFFER. The BUFFER flag goes high when the first data word is moved into the OUTPUT BUFFER. The DONE interrupt is pulsed when the complete message has been moved.
EXECUTE OP. WITH RPT OPTION	EXECUTES OPERATION SPECIFIED IN OPERATION REGISTER WITH REPEAT OPTION. 1. I/$\overline{O}$ BIT HIGH Data previously written into the INPUT BUFFER is loaded into a new INTERNAL RAM block specified by the T/R and SUBADDRESS field of the OPERATION REGISTER. This operation allows a block of data loaded in the INPUT BUFFER to be repeatedly copied into multiple subaddresses of the INTERNAL RAM without the subsystem having to reload the data. The done interrupt is pulsed when the operation is completed. The intent of the operation is to minimize the time required to initialize the INTERNAL RAM. 2. I/O BIT LOW Operation identical to EXECUTE OP. WITHOUT RPT option.

CT1800/1 HYBRID
MIL-STD-1553B BUS INTERFACE UNIT
FOR USE WITH CT1610/12 SERIES PROTOCOL HYBRID

PIN NUMBERS

Flat Pack	Plug In	Name	Function
44	44	+5V	Supply
77	79	GND	Return and Case
80	82	IH715 (MSB)	Internal Highway multiplexed Data Bus to/from CT1610/12 Hybrid
82	83	IH614	
83	84	IH513	
84	85	IH412	
85	86	IH311	
86	87	IH210	
87	88	IH19	
88	89	IH08 (LSB)	
33	33	$\overline{\text{NBGT}}$	Interface signals to/from CT1610/12 Hybrid including 6MHz system clock
28	28	$\overline{\text{INCMD}}$	
23	23	H/$\overline{\text{L}}$	
24	24	IUSTB	
21	21	$\overline{\text{SYNC}}$	
26	26	$\overline{\text{DTRQ}}$	
76	78	$\overline{\text{DTAK}}$	
22	22	$\overline{\text{GBR}}$	

PIN NUMBERS			
Flat Pack	Plug In	Name	Function
36	36	6MHZ	
75	77	$\overline{\text{BUSY}}$	
74	76	TX/$\overline{\text{RX}}$	
73	75	$\overline{\text{EOT}}$	
79	81	$\overline{\text{VECTEN}}$/$\overline{\text{DWEN}}$	
3	3	DBF (MSB)	I/O Data Bus for Subsystem Interface
4	4	DBE	
5	5	DBD	
6	6	DBC	
7	7	DBB	
8	8	DBA	
9	9	DB9	
10	10	DB8	
11	11	DB7	
12	12	DB6	
13	13	DB5	
14	14	DB4	
15	15	DB3	
16	16	DB2	

PIN NUMBERS			
Flat Pack	Plug In	Name	Function
17	17	DB1	
18	18	DBO (LSB)	
			Interface Signals
38	38	$\overline{\text{VALID TRANS}}$	Interrupt pulse, Transmit command.
39	39	$\overline{\text{SYNC NO DATA}}$	Interrupt pulse, SYNC w/o data mode command.
37	37	$\overline{\text{SYNC W/DATA}}$	Interrupt pulse, SYNC w/data mode command.
35	35	$\overline{\text{DONE}}$	Interrupt pulse, I/O load/unload buffer.
25	25	$\overline{\text{GOOD BLOCK}}$	Interrupt pulse, Receive command w/ valid data.
2	2	$\overline{\text{BUFF EF}}$	Monitor point, output buffer not empty on positive transition.
			Interface Signals
20	20	$\overline{\text{RD}}$	Input read strobe
19	19	$\overline{\text{WT}}$	Input write strobe
34	34	$\overline{\text{DS}}$	Input device select
29	29	ADO (LSB)	Input Address for OP code Interface signals.
30	30	AD1	
31	31	AD2	

PIN NUMBERS			
Flat Pack	Plug In	Name	Function
32	32	AD3 (MSB)	
78	80	$16/\overline{8}$	16 Bit/8 Bit I/O Data Bus programming pin
27	27	$\overline{\text{MASTER RESET}}$	System Reset
60	62	IB15 (MSB)	
59	61	IB14	
58	60	IB13	
57	59	IB12	Internal Bus with 10K Ohm pull down resitors. Test points and Data Bus to external RAM on CT1801 and CT 1802.
56	58	IB11	
55	57	IB10	
54	56	IB9	
53	55	IB8	
52	54	IB3	
51	53	IB6	
50	52	IB5	
49	51	IB4	
48	50	IB3	

PIN NUMBERS

Flat Pack	Plug In	Name	Function
70	72	A9	
71	73	A10 (MSB)	Note: A10 Function Low-->RCV buffer High->XMIT buffer used with 2Kx8 format external ram (1801/1802) when using separate RCV and XMIT sections.
72	74	AD10IN	Internal Address input (1800 only.) A10 generally connected to A10IN. If single XMIT/RCV buffer memory used, connect to logic high or low and not to A10.

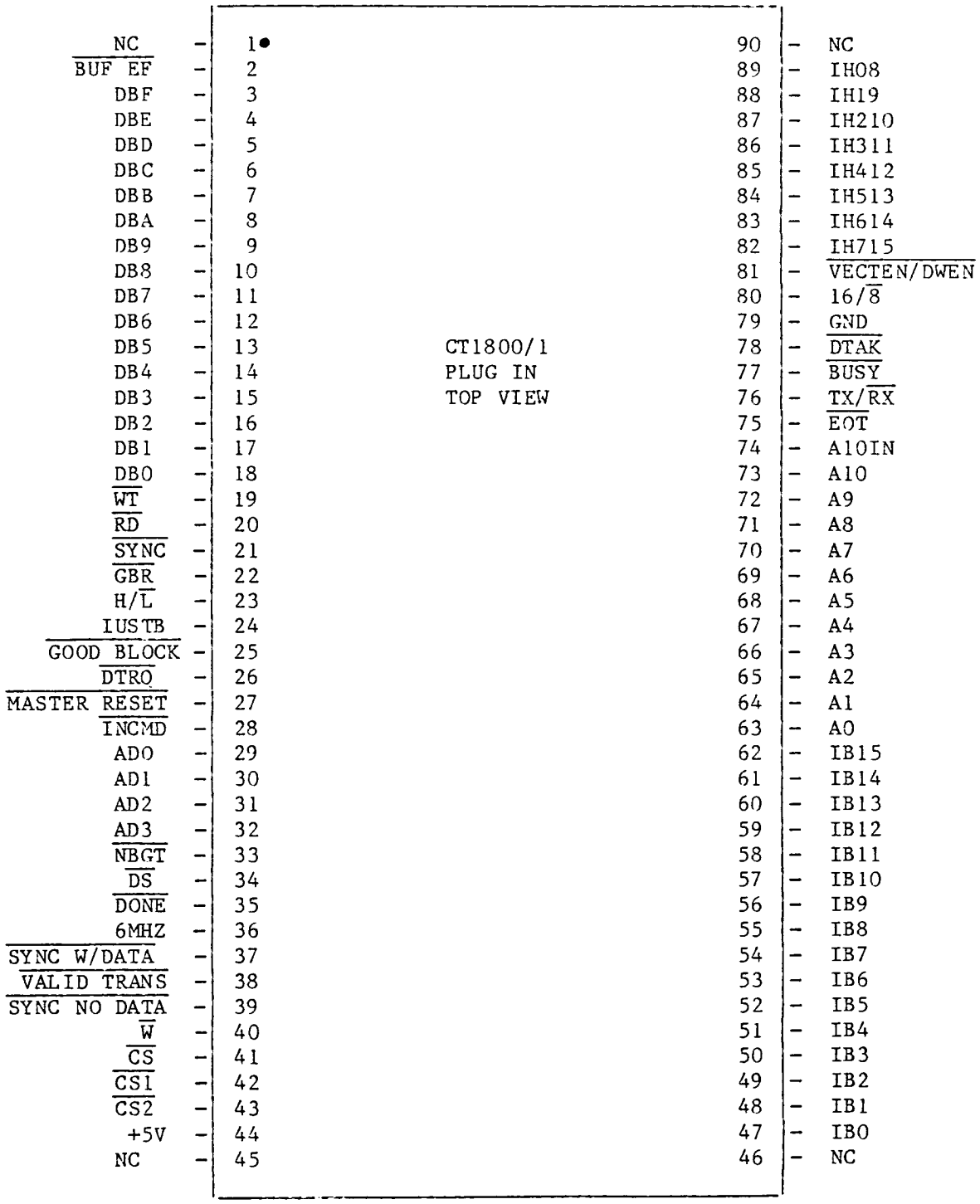
Total # Signal and Power Pins = 86

Total # Pins Plug in Package = 90
(CORNER PINS:1, 45, 46, 90 NOT USED)

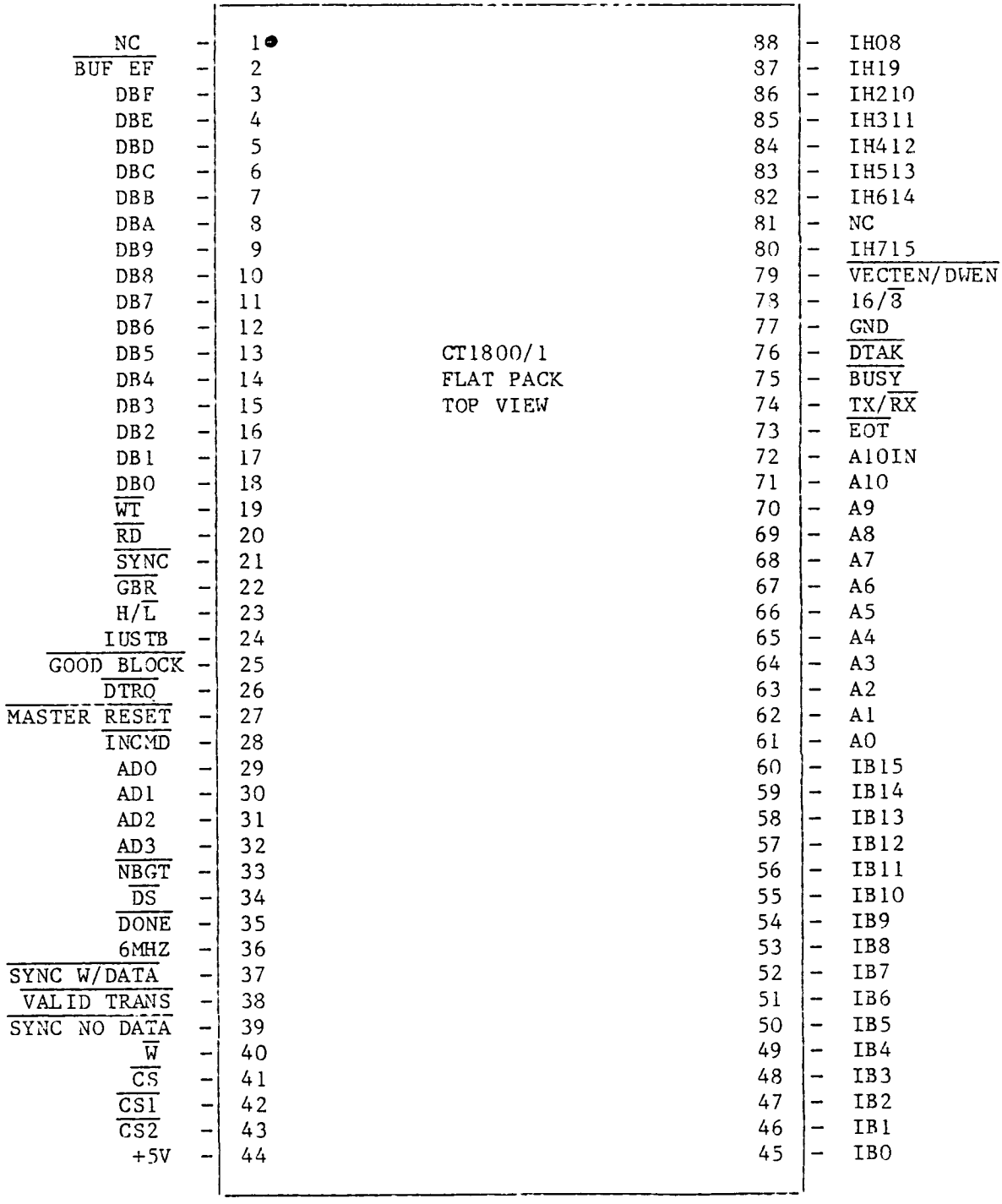
Total # Pins Flat Pack Package = 88
(PINS 1 AND 81 NOT USED)

PIN NUMBERS

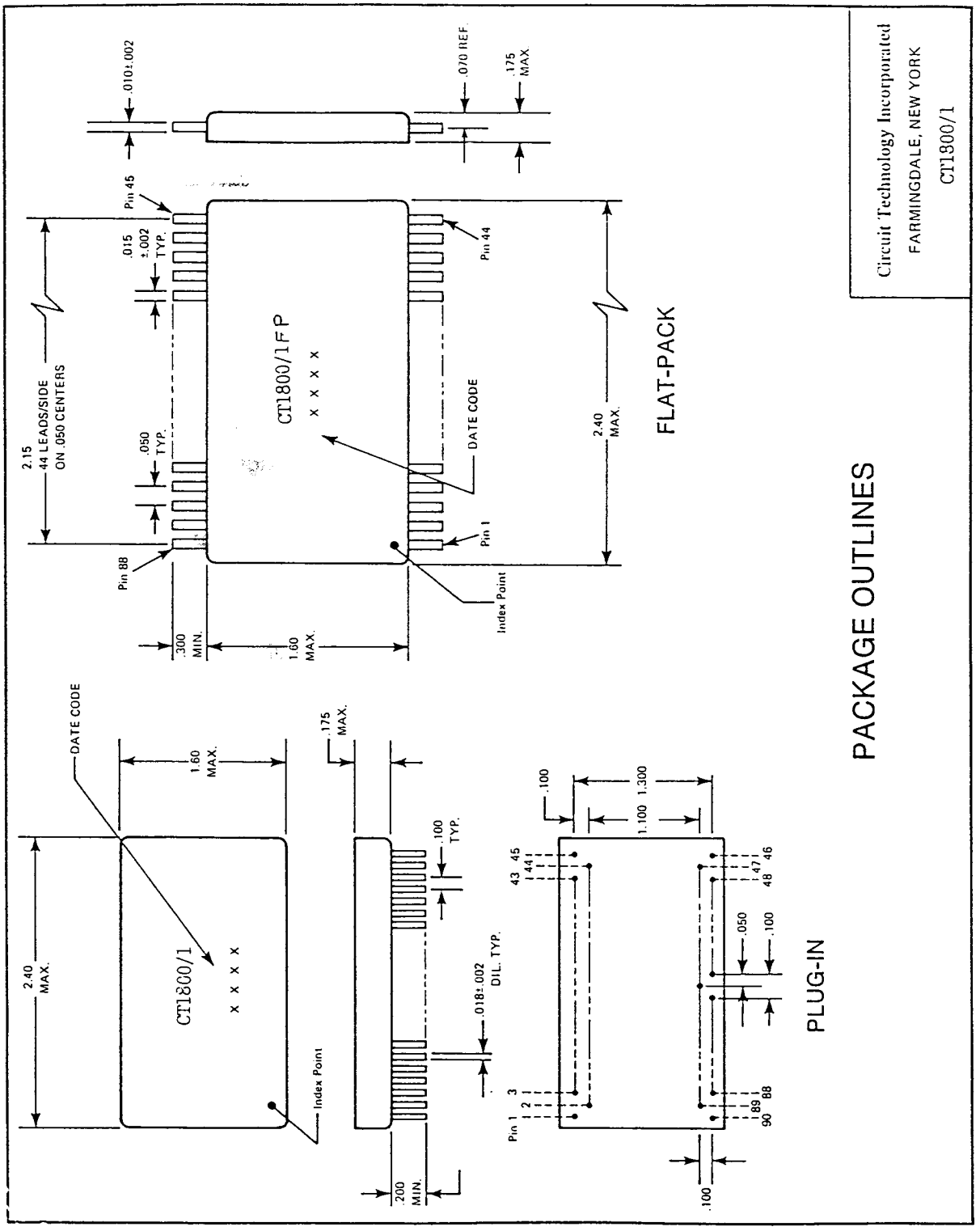
Flat Pack	Plug In	Name	Function
47	49	IB2	
46	48	IB1	
45	47	IB0 (LSB)	
40	40	$\overline{W}$	Test Point & Internal write strobe for use with external RAM (1801 & 1802)
41	41	$\overline{CS}$	Test Point & Internal chip select strobe(1801/1802)for 2Kx8 format RAM or common RVC/XMIT buffer.
42	42	$\overline{CS1}$	Test Point & 1801/1802 chip select for RVC buffer when using 1Kx4 6514 Type external RAM)
43	43	$\overline{CS2}$	Test point & 1801/1802 chip select for XMT buffer when using 1Kx4 6514 type external RAM)
61	63	A0 (LSB)	
62	64	A1	
63	65	A2	Internal address outputs (Used as address lines to external ram on 1801 and 1802)
64	66	A3	
65	67	A4	
66	68	A5	
67	69	A6	
68	70	A7	
69	71	A8	



NOTE: Pin 74 is NC on CT1801.



NOTE: Pin 72 is NC on CT1801FP.



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